

EGC220

Class Notes

5/5/2023

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Division of Engineering Programs

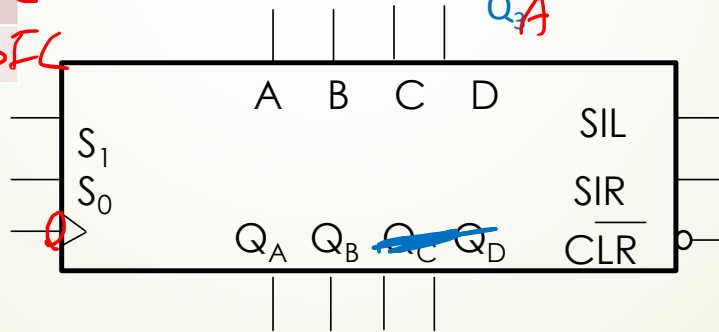
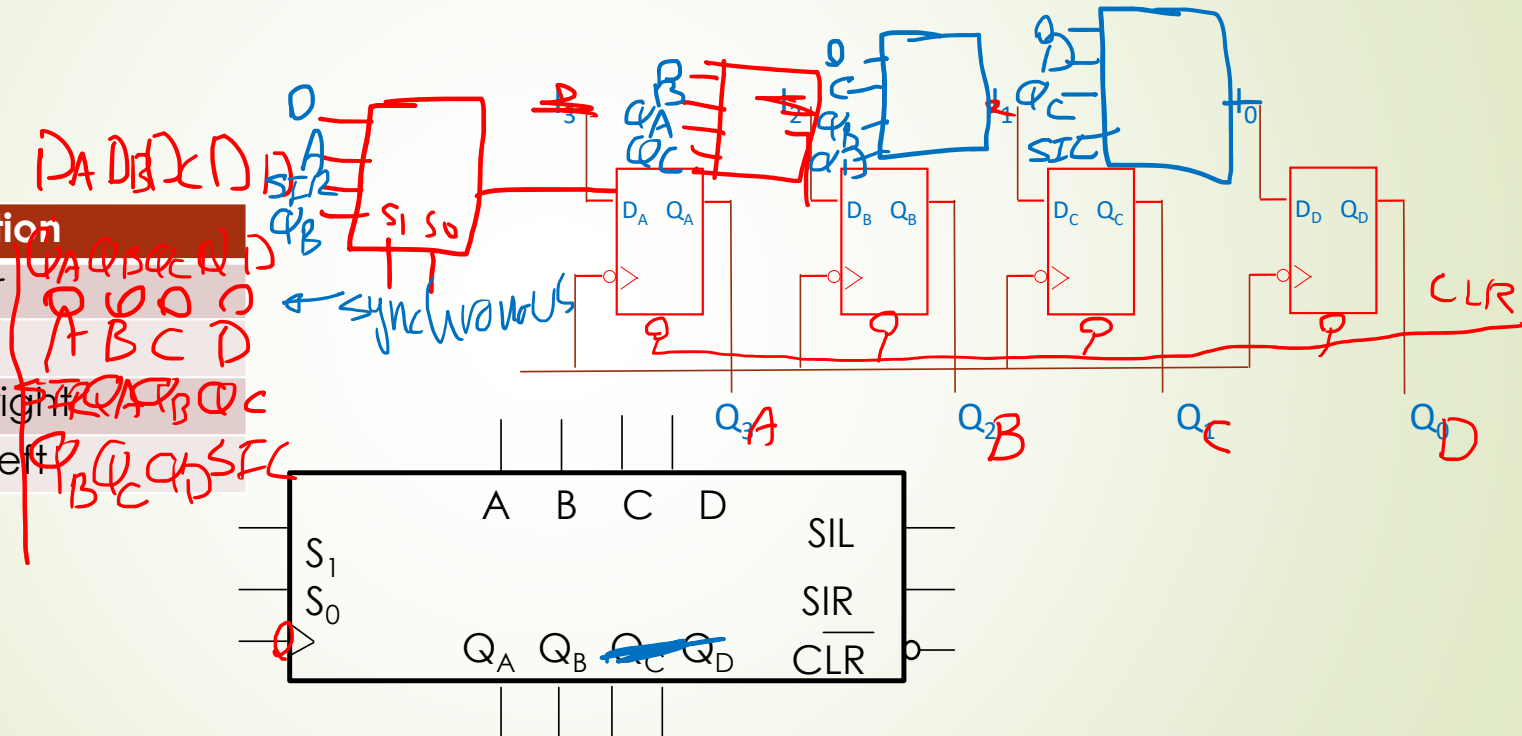
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Problem 7 (set 23)

Using D flip-flops and Multiplexers, design a 4-bit register with the following functionality

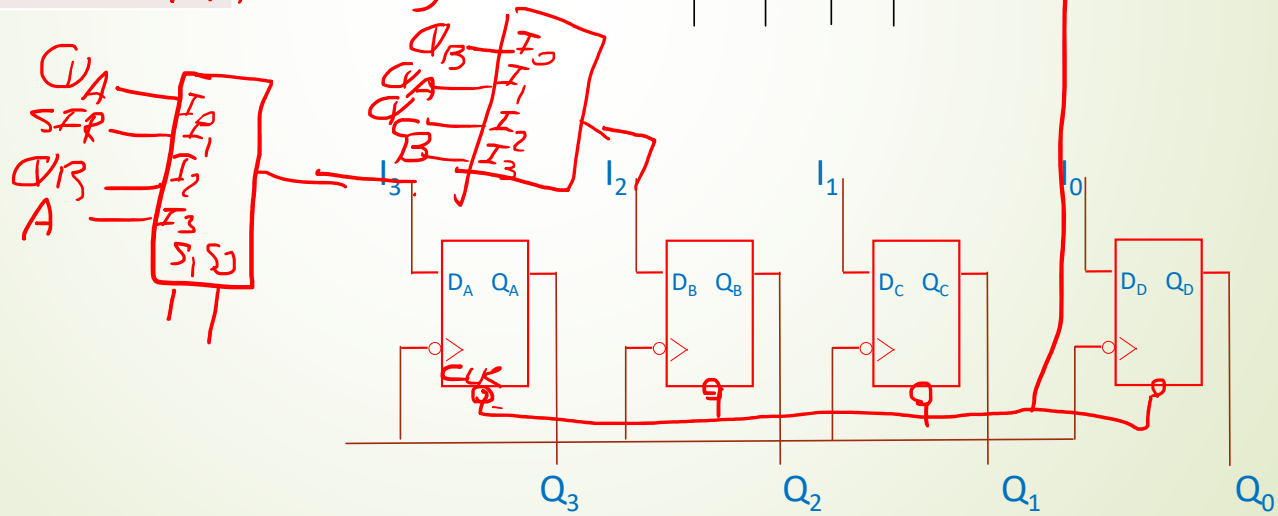
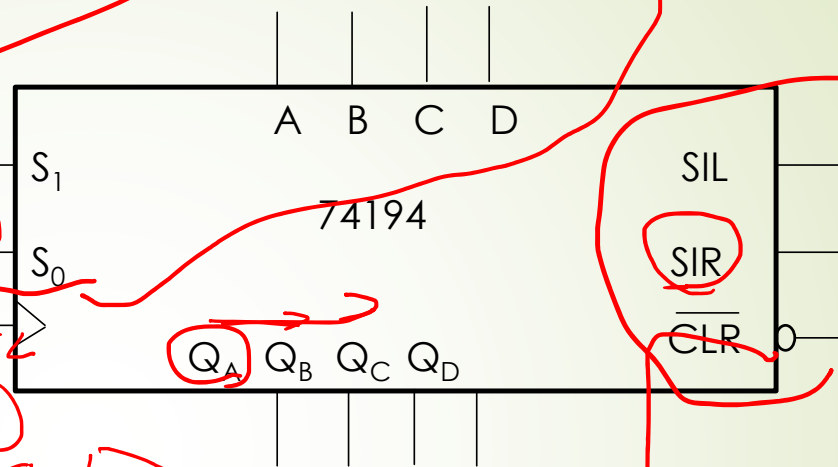
S1	S0	Function
0	0	Clear
0	1	load
1	0	Shift right
1	1	Shift left



74194 shift register

S_1	S_0	Function
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

$D_A D_B C D_D$
 $Q_A Q_B Q_C Q_D$
 $STR Q_A Q_B C$
 $Q_B Q_C Q_D SIL$
 $A B C D$



Problem 1

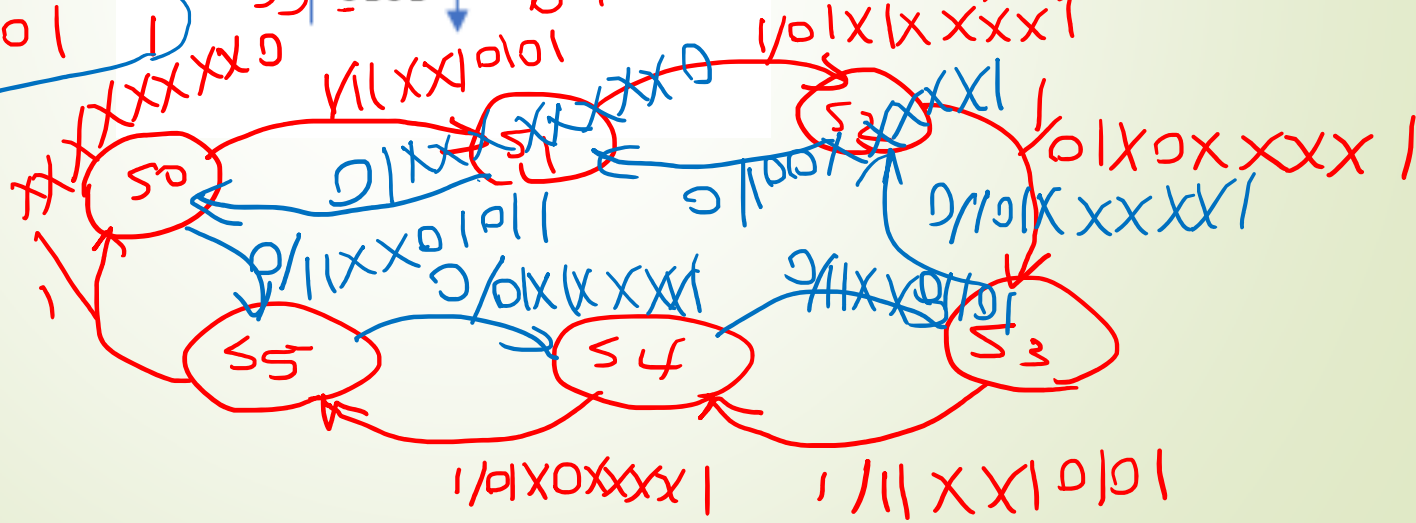
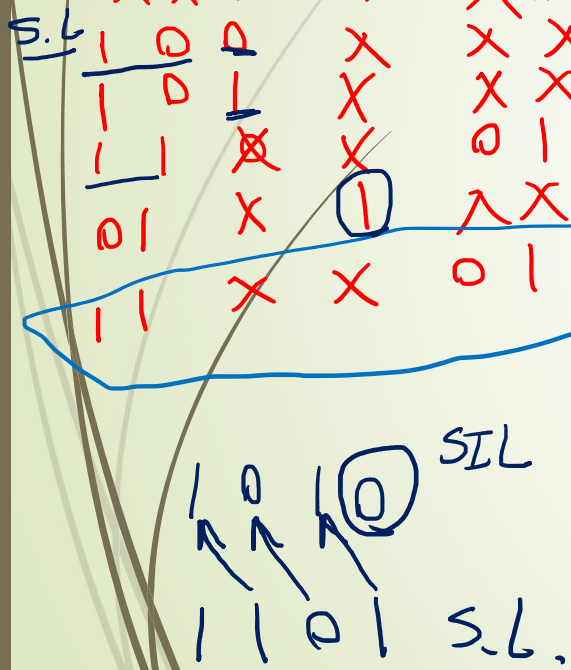
Using D flip-flops, design a Mealy based controller to generate the following sequence at the output of 74194

010X

x=0

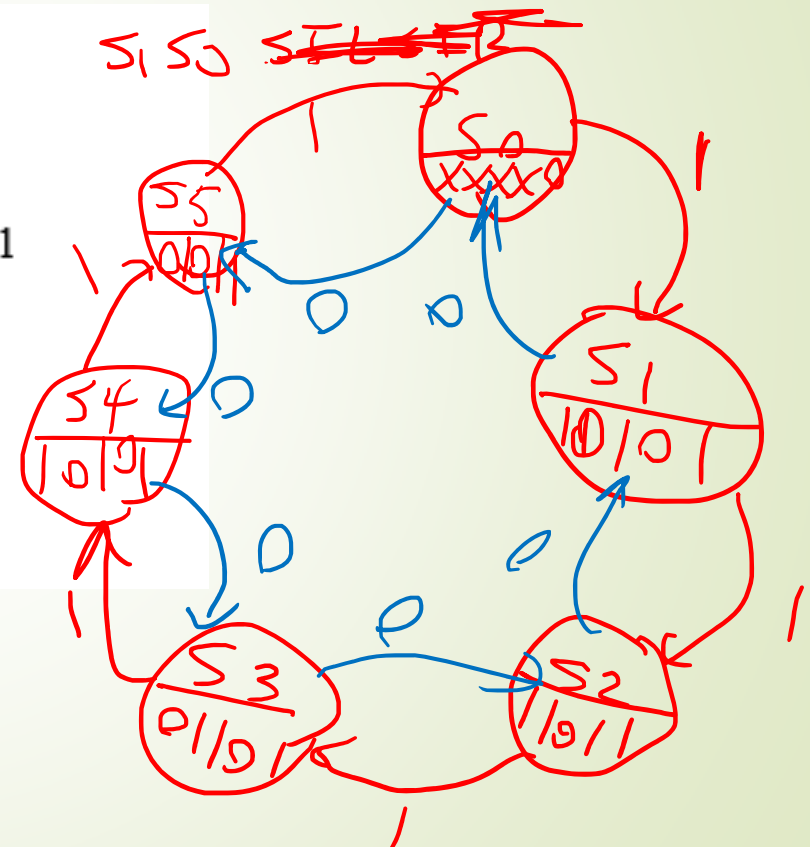
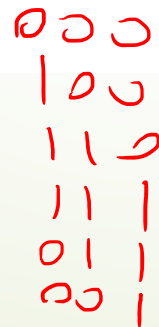
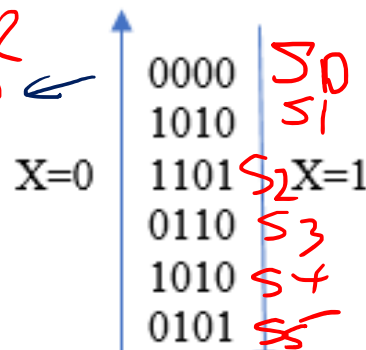
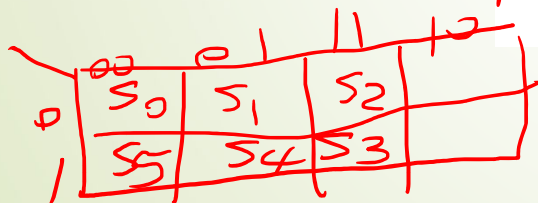
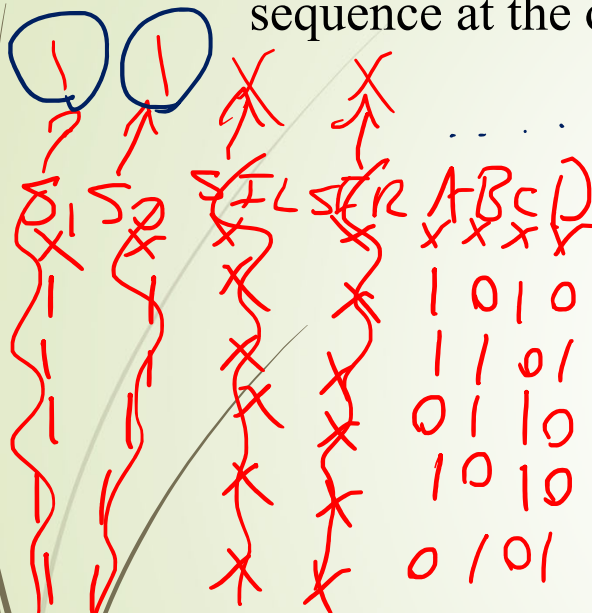
x=1

x=0							x=1										
S1	S0	SIL	SIR	A	B	C	D	CLR	S1	S0	SIL	SIR	A	B	C	D	CLR
X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0
1	0	0	X	X	X	X	X	1	1	1	X	X	1	0	1	0	1
1	0	1	X	X	X	X	X	1	0	1	X	0	X	X	X	X	1
1	1	X	X	0	1	1	0	1	0	1	X	X	1	0	1	0	1
0	1	X	1	X	X	X	X	1	0	1	X	0	X	X	X	X	1
1	1	X	X	0	1	0	1	1									



Problem 2

Using D flip-flops, design a Moore based controller to generate the following sequence at the output of 74194 *only load*

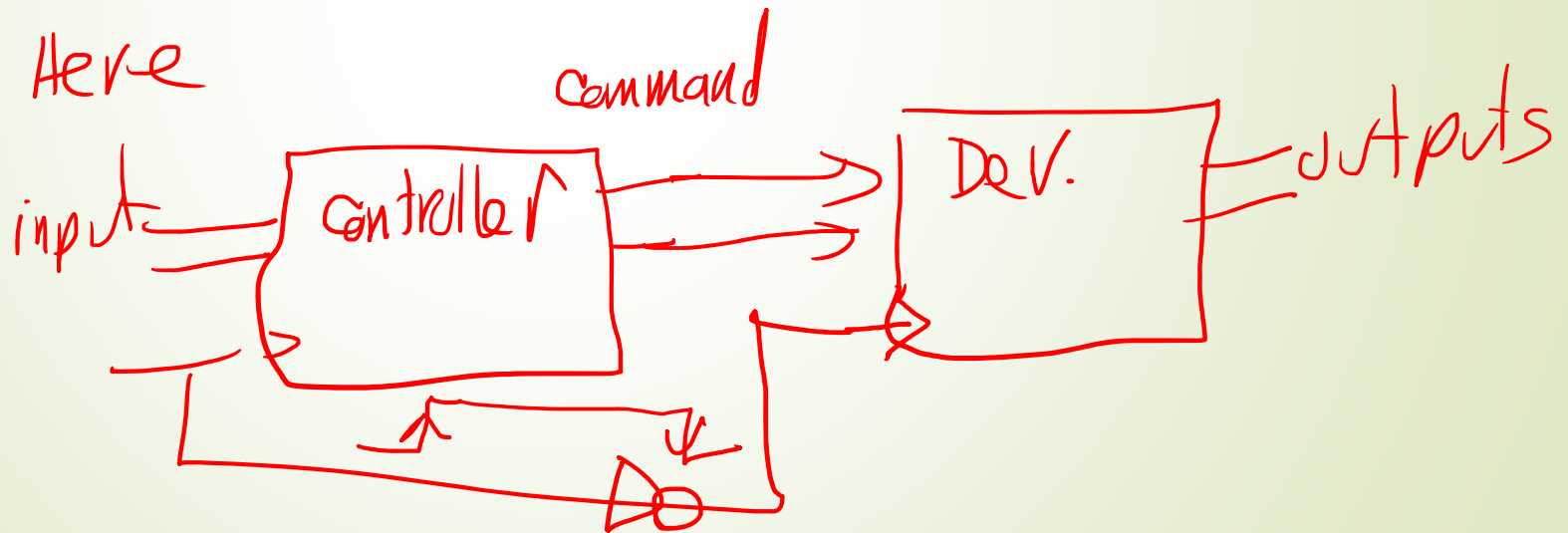


Before



Here

Program



Final

- Number systems
 - Simplification using K-map
 - SOP, POS, Standard SOP and POS, Min. SOP and POS
 - Design of combinational circuits
 - Circuit conversion to all NAND or NOR gates
 - Multiplexers, Demultiplexers, Decoders, Encoders
 - Design of combinational circuits using PLD's
- Latch and flip flops characteristics and excitation tables, design of ripple counters
 - Analysis of sequential circuits
 - Design of sequential circuits
 - Design using Mealy and Moore model
 - Design of a sequence detector
 - Design of a shift register
 - Design of a controller